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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,195	08/29/2000	Feng-Jong Edward Yang	F0255	8593

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EXAMINER	
BATES, KEVIN T	
ART UNIT	PAPER NUMBER
2155	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,195	YANG ET AL.	
	Examiner	Art Unit	
	Kevin Bates	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-13 and 15-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-13, and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

This Office Action is in response to a communication made on February 2, 2005.

Claims 1-7, 9-13, and 15-19 are pending in this application.

Response to Arguments

In view of the appeal filed on February 2, 2005, PROSECUTION IS HEREBY REOPENED. A new grounds of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10-11 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bass (6460120) in view of Humphrey (4933846).

Regarding claim 10, Bass discloses in a network device (Column 3, lines 36 – 42) that controls communication of data frames between stations (Column 4, lines 41 – 43), a method of storing data frame information (Column 7, lines 24 – 26), comprising: receiving a plurality of data frames; temporarily storing the received data frames in a plurality of receive devices (Column 7, lines 28 – 32), and simultaneously transferring data frame information to at least a first memory and a second memory (Column 25, lines 6 – 9), but does not explicitly indicate wherein the simultaneously transferring includes: alternately transferring data frame information from a first group of the receive devices to the first and second memories, and alternately transferring data frame information from a second group of the receive devices to the first and second memories. Humphrey discloses a network device configured to control communication of data frames between stations (Column 4, lines 60 – 66). Humphrey teaches transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the received devices to a second memory, the external memory interface includes a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory (Column 5, lines 5, lines 9 – 13) and alternately transferring data frame information from a first group of the receive devices to the first and second memories, and alternately transferring data frame information from a second group of the receive devices to the first and second memories (Column 5, lines 44 – 63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Humphrey's teachings in Bass' network device in order to allow multiple

devices and ports to communicate in the same device at a high throughput (Column 2, lines 56 – 62)

Regarding claim 11, the combination of Bass and Humphrey discloses simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively (Humphry, Column 5, lines 25 – 34).

Regarding claim 13, the combination of Bass and Humphrey discloses that simultaneously transferring further includes: sending a portion of a first data frame via a first external memory bus and sending a portion of a second data frame via a second external memory bus (Humphrey, Column 5, lines 5, lines 9 – 13; lines 25 – 34).

Regarding claim 15, the combination of Bass and Humphrey discloses that simultaneously retrieving data frame information from the first and second memories (Humphrey, Column 5, lines 19 – 21).

Claims 1-6, 9, 12, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bass (6460120) in view of Humphrey (4933846), and in further view of Mann (6021477).

Regarding claim 1, Bass discloses a network device (Column 3, lines 36 – 42) configured to control communication of data frames between stations (Column 4, lines 41 – 43), comprising: a plurality of receive devices corresponding to ports on the network device (Column 10, lines 17 – 22), the receive devices configured to receive data frames from the stations (Column 7, lines 24 – 26); an external memory interface (Column 9, lines 46 – 49) configured to receive data from the plurality of receive devices

(Column 9, lines 55 – 60), and a first and second memory (Column 7, lines 1 – 2), but Bass does not explicitly indicate to transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the received devices to a second memory, the external memory interface includes a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory, the external memory interface being further configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus. Humphrey discloses a network device configured to control communication of data frames between stations (Column 4, lines 60 – 66). Humphrey teaches transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the received devices to a second memory, the external memory interface includes a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory (Column 5, lines 5, lines 9 – 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Humphrey's teachings in Bass' network device in order to allow multiple devices and ports to communicate in the same device at a high throughput (Column 2, lines 56 – 62). Mann discloses a memory interface with dual memories (Figure 2a, elements 24, 28, and 30). Mann teaches a system that generates odd address information when transferring data to the first memory and even address information when transferring data via the second memory (Column 2, lines 38 – 44,

odd and even memories; Column 5, line 61 – Column 6, line 17, generating odd and even addresses). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Mann's teaching in Bass's system in order to allow fixed bus length systems work store information double that fixed bus length using dual memories (Column 1, lines 56 – 65).

Regarding claims 2, the combination of Bass, Mann, and Humphrey discloses that the external memory interface includes: a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories, the scheduler simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively (Humphry, Column 5, lines 25 – 34).

Regarding claims 3 and 12, the combination of Bass, Mann, and Humphrey discloses that the external memory interface is further configured to simultaneously transfer 8 bytes of data from the first receive device to the first memory and 8 bytes of data from the second receive device to the second memory (Humphrey, Column 5, lines 5, lines 9 – 13, for the simultaneous transfer; Mann, Column 1, lines 35 – 36; Column 2, lines 52 – 55 for the 8 bytes or 64 bits).

Regarding claim 4, the combination of Bass, Mann, and Humphrey discloses that the external memory interface is further configured to simultaneously transfer the protions of the data from the first and second receive devices to the first and second memories (Humphrey, Column 5, lines 5, lines 9 – 13; lines 25 – 34).

Regarding claim 5, the combination of Bass, Mann, and Humphrey discloses that the external memory interface is configured to simultaneously transfer data received from a first one of a first group of the receive devices via the first external memory bus and a second one of a second group of the receive devices via the second external memory bus (Humphrey, Column 5, lines 5 – 10; Mann, Column 2, lines 52 – 55).

Regarding claim 6, the combination of Bass, Mann, and Humphrey discloses that the external memory interface is further configured to alternately transfer data received from the first group of receive devices to the first and second memories and to alternately transfer data received from the second group of receive devices to the first and second memories (Humphrey, Column 5, lines 5, lines 9 – 13; lines 25 – 34; lines 39 – 54).

Regarding claim 9, the combination of Bass, Mann, and Humphrey discloses that the external memory interface is further configured to simultaneously retrieve data from the first and second memories (Humphrey, Column 5, lines 19 – 21).

Regarding claim 16, Bass discloses a data communication system for controlling the communication of data frames between stations, comprising: a plurality of receive devices configured to receive data frames from the stations, but does not explicitly indicate a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices; and a switching device configured to receive the data frame information and to simultaneously transfer data frame information from a first one of the data frames via a first external memory bus and data frame information from a second one of the data

frames via a second external memory bus; a first memory configured to receive data frame information from the first external memory bus; and a second memory configured to receive data frame information from the second external memory bus, wherein the switching device is further configured to: generate data address information having odd addresses for data transferred to the first memory and generate data address information having even addresses for data transferred to the second memory. Humphrey discloses a network device configured to control communication of data frames between stations (Column 4, lines 60 – 66). Humphrey teaches transfer a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the received devices to a second memory, the external memory interface includes a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory (Column 5, lines 5, lines 9 – 13) and a scheduler configured to generate selection signals to selectively output data frame information from the receive devices (Humphrey, Column 5, lines 25 – 34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Humphrey's teachings in Bass' network device in order to allow multiple devices and ports to communicate in the same device at a high throughput (Column 2, lines 56 – 62). Mann discloses a memory interface with dual memories (Figure 2a, elements 24, 28, and 30). Mann teaches a system that generates odd address information when transferring data to the first memory and even address information when transferring data via the second memory (Column 2, lines 38 – 44, odd and even memories; Column 5, line 61 – Column

6, line 17, generating odd and even addresses). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Mann's teaching in Bass's system in order to allow fixed bus length systems work store information double that fixed bus length using dual memories (Column 1, lines 56 – 65).

Regarding claim 17, the combination of Bass, Mann, and Humphrey discloses that there are first and second multiplexers coupled to first and second groups of the receive devices, respectively, each of the first and second multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame (Bass, Figure 1, elements 14 and 36).

Regarding claim 18, the combination of Bass, Mann, and Humphrey discloses that the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses (Humphrey, Column 5, lines 5, lines 9 – 13; lines 25 – 34; lines 39 – 54).

Regarding claim 19, the combination of Bass, Mann, and Humphrey discloses that the first memory is configured to store data words having odd addresses; and the second memory is configured to store data words having even addresses (Mann, Column 5, line 61 – Column 6, line 17).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hassell in view of Springer in further view of Gayton as applied to claims 1-6, 9, 12, and 16-19 above, and further in view of Runaldue (6052751) (Applicants IDS).

Regarding claim 7, the combination of Bass, Mann, and Humphrey discloses that the first and second external memory buses are each 8-bytes wide (Mann, Column 1, lines 35 – 36; Column 2, lines 52 – 55 for the 8 bytes or 64 bits), but does not explicitly indicate that the frequency is 100 MHz. Runaldo discloses that external memory can operate at 100 MHz (Column 5, line 32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Runaldo's teaching that external memory can operate at 100 MHz and enable Bass's switch to interface with memory at that speed.

Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No. 5875470 issued to Dreibelbis, because it discloses a plurality of receive devices and stations accessing a plurality of memory units with multiple buses.

U. S. Patent No. 5696913 issued to Gove, because it discloses multiprocessors addressing multiple memories independently.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Bates whose telephone number is (571) 272-3980. The examiner can normally be reached on 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571) 272-4001. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KB

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May 6, 2005

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